ABSTRACT OF THE DISCLOSURE

A method and apparatus for optimizing clock distribution in a circuit to reduce the effect of power supply noise. Parameters are determined including: a response curve of a power source for a circuit, a delay sensitivity of a clock net in the circuit to the power source, a delay sensitivity of a data net in the circuit to the power source, a data delay for the data net, and a clock delay for the clock net. The clock delay is adjusted to reduce the effect of power supply noise on the data net. The adjusting is based on the response curve of the power source, the delay sensitivity of the clock net, the delay sensitivity of the data net, the data delay, and the clock delay. The adjusting includes adding a pre-distribution clock delay.